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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Akram et al.

Serial No.: 10/032,734

Filed: December 28, 2001

For: MULTI-CHIP MODULE SYSTEM AND METHOD OF FABRICATION

Examiner: Unknown

Group Art Unit: 2812

Attorney Docket No.: 2754.4US (95-0742.4)

CERTIFICATE OF MAILING

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PRELIMINARY AMENDMENT

Box Non-Fee Amendment
Commissioner for Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-referenced patent application on the merits, entry of the amendments as set forth herein is respectfully solicited.

IN THE CLAIMS:

Claims 1-10, 16-28 and 34-36 have been amended herein. All of the pending claims 1 through 36 are presented, pursuant to 37 C.F.R. §§ 1.121(c)(1)(i) and 1.121(c)(3), in clean form below. Please enter these claims as amended. Also attached is a marked-up version of the claims amended herein pursuant to 37 C.F.R § 1.121(c)(1)(ii).

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1. (Amended) A multi-chip module system comprising:

a substrate having at least a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat and having at least one other vacant position having, in turn, a predetermined configuration for locating a second semiconductor device thereat on the multi-chip module system; and

a first semiconductor device located in the at least first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic.

2. (Amended) The multi-chip module system of claim 1, further comprising:

the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat which is substantially the same as the first semiconductor device.

3. (Amended) The multi-chip module system of claim 1, further comprising:

the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat; and

the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

4. (Amended) The multi-chip module system of claim 1, further comprising:

the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat; and

the second semiconductor device having a second predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

5. (Amended) A multi-chip module system comprising:

a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, and having at least one other vacant position having, in turn, a predetermined configuration for locating a third semiconductor device thereat on the multi-chip module system;

the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.

6. (Amended) The multi-chip module system of claim 4, further comprising:

the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat which is substantially the same as the first semiconductor device.

7. (Amended) The multi-chip module system of claim 4, further comprising:

the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and

the third semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first

semiconductor device.

8. (Amended) The multi-chip module system of claim 4, further comprising:
the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and
the third semiconductor device having a predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

9. (Amended) The multi-chip module system of claim 4, further comprising:
the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and
the third semiconductor device having a predetermined performance characteristic of at least substantially three times greater than that of the second predetermined performance characteristic of the second semiconductor device.

10. (Amended) The multi-chip module system of claim 4, further comprising:
the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and
the third semiconductor device having a predetermined performance characteristic of at least substantially four times greater than that of the first and the second predetermined performance characteristic of the first semiconductor device and the second semiconductor device combined.

11. The multi-chip module system of claim 4, wherein the first semiconductor device comprises a memory device.

12. The multi-chip module system of claim 4, wherein the second semiconductor device comprises a memory device.

13. The multi-chip module system of claim 4, wherein the first semiconductor device comprises a microprocessor device.

14. The multi-chip module system of claim 4, wherein the second semiconductor device comprises a microprocessor device.

15. The multi-chip module system of claim 4, wherein the multi-chip module system comprises a single in-line memory module system.

16. (Amended) The multi-chip module system of claim 4, further comprising:
a third semiconductor device; and
an adapter connected to the third semiconductor device, the adapter having a configuration for connecting the adapter to the at least one other vacant position on the substrate to connect the third semiconductor device to the substrate.

17. (Amended) A multi-chip module system comprising:
a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, having a first vacant position having, in turn, a predetermined configuration for locating a third semiconductor device thereat, and having a second vacant position having, in turn, a predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system;
the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and
the second semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.

18. (Amended) The multi-chip system module of claim 17, wherein:
the first vacant position located on the substrate is located on one side of the substrate; and
the second vacant position located on the substrate is located on the other side of the substrate.

19. (Amended) A multi-chip module system comprising:
a substrate having at least a first predetermined configuration position for locating a first semiconductor device thereat and having at least one other vacant predetermined configuration position for locating a second semiconductor device thereat on the multi-chip module system; and
the first semiconductor device located in the at least the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic.

20. (Amended) The multi-chip module system of claim 19, further comprising:
the at least one other vacant predetermined configuration position for locating the second semiconductor device thereat which is substantially the same as the first semiconductor device.

21. (Amended) The multi-chip module system of claim 19, further comprising:
the at least one other vacant predetermined configuration position having a predetermined configuration for locating the second semiconductor device thereat; and
the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

22. (Amended) The multi-chip module system of claim 19, further comprising:

the at least one other vacant predetermined configuration position having a predetermined configuration for locating the second semiconductor device thereat; and

the second semiconductor device having a predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

23. (Amended) A multi-chip module system comprising:

a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, and having at least one other vacant predetermined configuration position for locating a third semiconductor device thereat on the multi-chip module system;

the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.

24. (Amended) The multi-chip module system of claim 23, further comprising:

the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat which is substantially the same as the first semiconductor device.

25. (Amended) The multi-chip module system of claim 23, further comprising:
the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat; and
the third semiconductor device having a third predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

26. (Amended) The multi-chip module system of claim 23, further comprising:
the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat; and
the third semiconductor device having a third predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

27. (Amended) The multi-chip module system of claim 23, further comprising:
the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat; and
the third semiconductor device having a third predetermined performance characteristic of at least substantially three times greater than that of the second predetermined performance characteristic of the second semiconductor device.

28. (Amended) The multi-chip module system of claim 23, further comprising:
the at least one other vacant predetermined configuration position for locating a third semiconductor device thereat; and
the third semiconductor device having a third predetermined performance characteristic of at least substantially four times greater than that of the first and second predetermined performance characteristic of the first semiconductor device and the second semiconductor device combined.

29. The multi-chip module system of claim 23, wherein the first semiconductor device comprises a memory device.

30. The multi-chip module system of claim 23, wherein the second semiconductor device comprises a memory device.

31. The multi-chip module system of claim 23, wherein the first semiconductor device comprises a microprocessor device.

32. The multi-chip module system of claim 23, wherein the second semiconductor device comprises a microprocessor device.

33. The multi-chip module system of claim 23, wherein the multi-chip module system comprises a single in-line memory module system.

34. (Amended) The multi-chip module system of claim 23, further comprising:
an adapter connected to the third semiconductor device, the adapter for connecting the adapter to the at least one other vacant predetermined configuration position on the substrate to connect the third semiconductor device to the substrate.

35. (Amended) A multi-chip module system comprising:
a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, having a first vacant predetermined configuration position for locating a third semiconductor device thereat, and having a second vacant predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system;
the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and

the second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic.

36. (Amended) The multi-chip module of claim 35, wherein:

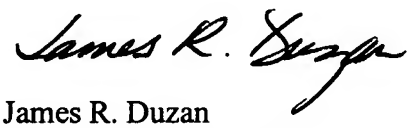
the first vacant predetermined configuration position located on the substrate is located on one side of the substrate; and

the second vacant predetermined configuration position located on the substrate is located on the other side of the substrate.

REMARKS

No new matter has been added. The Applicants again request entry of the amendments as set forth in the Appendices hereto prior to examination of the application on the merits.

Respectfully submitted,



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Enclosure: Version of Claims with Markings to Show Changes Made